

REMARKS

Claims 1 and 30 are amended hereby. No claims have been added or canceled. Claims 34-38 have been withdrawn from further consideration. As a result, claims 1-33 remain under consideration.

In the Office Action, the Examiner set forth the Restriction Requirement that was discussed with the undersigned on March 15, 2005. Specifically, the Examiner identified two groups of invention: (1) Group I, encompassing claims 1-33, drawn to a method for forming a microstructure, and (2) Group II, encompassing claims 34-38, drawn to a processing tool. As stated by the Examiner, the Applicant verbally elected Group I for further prosecution, without traverse, on March 15, 2005. The Applicant confirms that election hereby.

In the Office Action, the Examiner objected to claim 31 because the claim, as formerly presented, was dependent upon itself. The Applicant has amended claim 31 to depend from claim 30. Accordingly, the Applicant respectfully requests that the Examiner withdraw the objection to claim 31.

Claims 1-5, 10-12, 15-19, and 21-29 were rejected under 35 U.S.C. § 102(b) as anticipated by Maiti et al. (U.S. Patent No. 6,020,024). The Examiner also rejected claims 6-9, 13-14, 20, and 30-33 under 35 U.S.C. § 103(a) as unpatentable over Maiti et al. in view of Ballantine et al. (U.S. Patent No. 6,444,592). The Applicant respectfully disagrees with both rejections and, therefore, respectfully traverses same.

Maiti et al. describes a method for forming high dielectric constant metal oxides. Maiti et al. discusses a substrate 12 that has been pre-cleaned to minimize the oxide at its surface. (Maiti et al. at col. 2, lines 61-67.) After the substrate 12 is cleaned, the substrate 12 is exposed to a nitridation agent 13 to form a thin nitrided layer 14. (Maiti et al. at col. 3, lines 1-22, and Fig. 1.) The metal oxide gate layer 16

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is formed by the deposition 18 of a metal film followed by an oxidizing ambient. (Maiti et al. at col. 3, lines 30-33, and Fig. 2.) Therefore, the final structure formed by Maiti et al. has a substrate 12 with a nitrided layer 14 thereon. The metal oxide layer 16 sits atop the nitrided layer 14.

At no point does Maiti et al. discuss or suggest, among other things, performing an oxidation process during and/or after said depositing wherein an interfacial oxide layer is grown between the diffusion filter layer and the substrate, the interfacial oxide layer growth being controlled by the diffusion coefficient of the diffusion filter layer. Since Maiti et al. does not describe each and every feature as recited by claims 1-33, the reference cannot be relied upon to anticipate those claims.

Ballantine et al. does not assist the Examiner in fashioning a rejection of the claims. Ballantine et al. describes an interfacial oxidation process for high-k dielectric process integration. As discussed by Ballantine et al., the semiconductor structure includes a semiconductor substrate 10 with an active device region 12 therein. (Ballantine et al., at col. 3, lines 21-32.) The active device region 12 includes an region in which electrons are allowed to flow freely. (Ballantine et al., at col. 3, lines 50-51.) An ultra-thin oxide, oxynitride, and/or nitride layer 14 is formed on the substrate 10. (Ballantine et al., at col. 3, lines 59-67.) The high-k dielectric layer 16 is formed on the oxide/oxynitride/nitride layer 14. Ballantine et al. does not discuss or suggest performing an oxidation process during and/or after said depositing wherein an interfacial oxide layer is grown between the diffusion filter layer and the substrate. Accordingly, Ballantine et al. cannot be combined with Maiti et al. to render obvious the claims.

The Applicant respectfully submits that the references relied upon by the Examiner do not, either alone or in combination, describe or suggest the invention as

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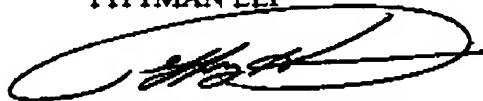
recited by claims 1-33. As a result, the Applicant respectfully submits that the claims are patentable over the references cited.

In view of the above amendments and remarks, Applicants respectfully submit that all of the claims are allowable and that the entire application is in condition for allowance.

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,  
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